

Page 243, replace line 13 as follows: --regarded as a special kind of the interface-board packaging.--.

In the Claims:

Please cancel claims 1-23.

Please add claims 24-49 as follows:

~~--24.~~ A switching fabric comprising
N/D P×M input nodes having output ports,
M/D N×Q output nodes having input ports, and
an interstage exchange interconnecting each one of the input nodes to each one of the output nodes with D lines, each of the lines interconnecting a distinct one of the output ports and a distinct one of the input ports, where $D > 1$, and D is a common factor of M and N.

25. The switching fabric as recited in claim 24 wherein $M = 2^{n-r}$, $N = 2^r$, and $D = 2^d$, with $1 < r < n$ and $1 \leq d < \min(r, n-r)$.

26. The switching fabric as recited in claim 25 wherein the interstage exchange is a bit-permuting exchange induced by a permutation π on integers from 1 to $n-d$ such that

the images of the numbers $r-d+1, r-d+2, \dots, n-d$ cover the numbers $1, 2, \dots, n-r-d$, or equivalently, the images of the numbers $1, 2, \dots, r-d$ are covered by the numbers $n-r-d+1, n-r-d+2, \dots, n-d$.

27. The switching fabric as recited in claim 26 wherein $P = 2^{n-r}$ and $Q = 2^r$.

28. The switching fabric as recited in claim 27 wherein each one of the input nodes is constructed from a k_1 -stage $2^{n-r} \times 2^{n-r}$ bit-permuting network of cells and each one of the output nodes is constructed from a k_2 -stage $2^r \times 2^r$ bit-permuting network of cells such that the switching fabric is a k -stage $2^{n-d} \times 2^{n-d}$ bit-permuting network of cells with $k=k_1+k_2$.

29. The switching fabric as recited in claim 28 wherein the trace and the guide of the k -stage bit-permuting network are respectively a k -term sequence containing the numbers from 1 to $n-d$.

30. The switching fabric as recited in claim 29 wherein each of the $D=2^d$ lines is replaced by a bundle of b lines, $b>1$, and each of the cells is dilated proportionately.

31. A switching network constructed from recursive 2-stage construction, one of the recursive steps constructing a modified 2-stage interconnection network, the modified 2-stage interconnection network comprising

N/D $P \times M$ input nodes having output ports,

M/D N×Q output nodes having input ports, and
 an interstage exchange interconnecting each one of the input nodes to each
 one of the output nodes with D lines, each of the lines interconnecting a distinct one of
 the output ports and a distinct one of the input ports, where $D > 1$, and D is a common
 factor of M and N.

32. The switching network as recited in claim 31 wherein $M = 2^{n-r}$, $N = 2^r$, and $D = 2^d$, with $1 < r < n$ and $1 \leq d < \min(r, n-r)$.

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33. The switching network as recited in claim 32 wherein the interstage exchange
 is a bit-permuting exchange induced by a permutation π on integers from 1 to $n-d$ such
 that the images of the numbers $r-d+1, r-d+2, \dots, n-d$ cover the numbers $1, 2, \dots, n-r-d$,
 or equivalently, the images of the numbers $1, 2, \dots, r-d$ are covered by the numbers
 $n-r-d+1, n-r-d+2, \dots, n-d$.

34. The switching network as recited in claim 33 wherein $P = 2^{n-r}$ and $Q = 2^r$.

35. The switching network as recited in claim 34 wherein each one of the input
 nodes is constructed from a k_1 -stage $2^{n-r} \times 2^{n-r}$ bit-permuting network of cells and each
 one of the output nodes is constructed from a k_2 -stage $2^r \times 2^r$ bit-permuting network of
 cells such that the modified 2-stage interconnection network is a k -stage $2^{n-d} \times 2^{n-d}$ bit-
 permuting network of cells with $k = k_1 + k_2$.

36. The switching network as recited in claim 35 wherein the trace and the guide of the k-stage $2^{n-d} \times 2^{n-d}$ bit-permuting network are respectively a k-term sequence containing the numbers from 1 to n-d.

37. The switching fabric as recited in claim 36 wherein each of the $D=2^d$ lines is replaced by a bundle of b lines, $b>1$, and each of the cells is dilated proportionately.

38. A switch based upon a plurality of opto-electrical-physical implementation levels comprising

A15 N/D first switching elements, each having P input ports and M output ports and having a configuration based on a first one of the implementation levels,

M/D second switching elements, each having N input ports and Q output ports and having a configuration based on a second one of the implementation levels, and

an interface circuit, which is compatible with both the first implementation level and the second implementation level, interconnecting each of the first switching elements to each of the second switching elements with D lines, each line interconnecting a distinct one of the output ports of the first switching elements and a distinct one of the input ports of the second switching elements, where $D > 1$, and D is a common factor of M and N.

39. The switch as recited in claim 38 wherein the interface circuit has MN/D input ports to cooperatively interconnect with the MN/D outputs of the N/D first switching elements, MN/D output ports to cooperatively interconnect with the MN/D inputs of the M/D second switching elements, and interconnections between the MN/D

input ports of the interface circuit and the MN/D output ports of the interface circuit corresponding to a pre-determined interstage exchange.

40. The switch as recited in claim 39 wherein the N/D first switching elements are arranged as a first stack of N/D parallel planes and the M/D second switching elements are arranged as a second stack of M/D parallel planes orthogonal to the first stack of planes.

41. The switch as recited in claim 38 wherein the interface circuit includes the first one, or the second one, or both the first one and the second one of the following circuitries:

115 (a) N/D first circuitries, each having M input ports to interconnect with the M output ports of a distinct one of the N/D first switching elements, and M output ports grouped into M/D output groups where each output group has D output ports,

(b) M/D second circuitries, each having N output ports to interconnect with the N input ports of a distinct one of the M/D second switching elements, and N input ports grouped into N/D input groups where each input group has D input ports, and

wherein the interface circuit further connects each output group of each one of the first circuitries to a distinct input group of a distinct one of the second circuitries.

42. The switch as recited in claim 41 wherein each one of the N/D first circuitries corresponds to an output exchange of a distinct one of the N/D first switching elements,

and each one of the M/D second circuitries corresponds to an input exchange of a distinct one of the M/D second switching elements.

43. The switching network as recited in claim 38 wherein $M = P = 2^{n-r}$, $N = Q = 2^r$, and $D = 2^d$, with $1 < r < n$ and $1 \leq d < \min(r, n-r)$.

44. The switching network as recited in claim 43 wherein each of the $D = 2^d$ lines is replaced by a bundle of b lines, $b > 1$, and each of the switching elements is dilated proportionately.

45. A switch comprising

N/D first switching elements arranged as a first stack of N/D parallel planes, each having P input ports and M output ports,

M/D second switching elements arranged as a second stack of M/D parallel planes orthogonal to the first stack of planes, each having N input ports and Q output ports, where $D > 1$, and D is a common factor of M and N ,

a plurality of first adaptors, wherein every D output ports of each one of the N/D first switching elements are adapted by a first adaptor into a single bundle of D output ports such that each one of the first switching elements has M/D bundles of D output ports, and

a plurality of second adaptors, wherein every D input ports of each one of the M/D second switching elements are adapted by a second adaptor into a single bundle of D input ports such that each one of the second switching elements has N/D bundles of D input ports, and wherein each one of the first switching elements is connected to each

one of the second switching elements by the connection of a distinct one of the M/D bundles of output ports and a distinct one of the N/D bundles of input ports.

46. A method for routing a packet through a $2^{n-d} \times 2^{n-d}$ k-stage bit-permuting network constructed from modified 2-stage interconnection, the packet having a destination address expressed as $D_1 D_2 \dots D_{n-d}$, the network including $2^{r-d} 2^{n-r} \times 2^{n-r}$ input nodes, $2^{n-r-d} 2^r \times 2^r$ output nodes, and an interstage exchange induced by a permutation π on integers from 1 to $n-d$ such that the images of the numbers $r-d+1, r-d+2, \dots, n-d$ cover the numbers $1, 2, \dots, n-r-d$, or equivalently, the images of the numbers $1, 2, \dots, r-d$ are covered by the numbers $n-r-d+1, n-r-d+2, \dots, n-d$, for $1 < r < n$ and

$1 \leq d < \min(r, n-r), k > n-d$, the method comprising

generating a routing tag for the packet from the destination address

$D_1 D_2 \dots D_{n-d}$ and the guide of the network expressed as $\gamma(1), \gamma(2), \dots, \gamma(k)$, the routing tag being a k-symbol string $D_{\gamma(1)} D_{\gamma(2)} \dots D_{\gamma(k)}$, and

routing the packet at the j-th stage using $D_{\gamma(j)}$ in the routing tag, $1 \leq j \leq k$.

47. The method as recited in claim 46 wherein, whenever $\gamma(p) = \gamma(q)$ in the guide of the network, where $p < q$, or equivalently, the p-th symbol of the routing tag $D_{\gamma(p)}$ is equal to the q-th symbol $D_{\gamma(q)}$, where $p < q$, disabling the whole stage of switching nodes at either stage-p or stage-q.

48. A method for routing a packet through a $2^{n-d} \times 2^{n-d}$ k-stage bit-permuting network constructed from modified 2-stage interconnection, the packet having a

rectangular set of destination addresses expressed as $Q_1 Q_2 \dots Q_{n-d}$, the network including $2^{r-d} 2^{n-r} \times 2^{n-r}$ input nodes, $2^{n-r-d} 2^r \times 2^r$ output nodes, and an interstage exchange induced by a permutation π on integers from 1 to $n-d$ such that the images of the numbers $r-d+1$, $r-d+2$, ..., $n-d$ cover the numbers 1, 2, ..., $n-r-d$, or equivalently, the images of the numbers 1, 2, ..., $r-d$ are covered by the numbers $n-r-d+1$, $n-r-d+2$, ..., $n-d$, for $1 < r < n$ and $1 \leq d < \min(r, n-r)$, $k > n-d$, the method comprising

generating a routing tag for the packet from the rectangular set of destination addresses $Q_1 Q_2 \dots Q_{n-d}$ and the guide of the network expressed as $\gamma(1)$, $\gamma(2)$, ..., $\gamma(k)$, the routing tag being a k -symbol string $Q_{\gamma(1)} Q_{\gamma(2)} \dots Q_{\gamma(k)}$,

whenever $\gamma(p) = \gamma(q)$ in the guide of the network, where $p < q$, disabling the multicasting function of the whole stage of switching nodes at either stage- p or stage- q , and routing the packet at the j -th stage using $Q_{\gamma(j)}$ in the routing tag, $1 \leq j \leq k$.

49. A method for constructing a switch based upon a plurality of opto-electrical-physical implementation levels, the method comprising

configuring N/D first switching elements based on a first one of the implementation levels, each of the first switching elements having P input ports and M output ports,

configuring M/D second switching elements based on a second one of the implementation levels, each of the second switching elements having N input ports and Q output ports, and

configuring an interface circuit, which is compatible with both the first implementation level and the second implementation level, to realize the interconnection

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between the first switching elements and the second switching elements such that each of the first switching elements is connected to each of the second switching elements with D lines, each line interconnecting a distinct one of the output ports of the first switching elements and a distinct one of the input ports of the second switching elements, where $D > 1$, and D is a common factor of M and N --.
